CLAIM LISTING:

1-7. (Cancelled)

8. (Currently Amended) A system for displaying frames, said system comprising:

a rasterizing circuit for rasterizing a first frame;

a controller for providing information regarding a second frame to the rasterizing circuit , after the ~~display engine~~ rasterizing circuit provides the first frame; and

wherein the rasterizing circuit rasterizes the first frame, if the controller does not provide the information regarding the second frame to the rasterizing circuit before a first horizontal synchronization pulse following a vertical synchronization pulse associated with the second frame.

9. (Previously Presented) The system of claim 8, wherein the rasterizing circuit rasterizes the second frame if the controller provides the information regarding the second frame before the first horizontal synchronization pulse following the vertical synchronization pulse associated with the second frame.

10. (Cancelled)

11. (Previously Presented) The system of claim 8, further comprising:

a frame buffer for storing the second frame beginning at at least one starting address; and

wherein the information regarding the second frame comprises the at least one starting address.

12. (Currently Amended) The system of claim 8, further comprising:

a first at least one register for storing ~~the~~ information regarding the first frame.

13. (Previously Presented) The system of claim 12, wherein the rasterizing circuit rasterizes the first frame based on the information regarding the first frame if the controller does not provide the information regarding the second frame before the first horizontal synchronization pulse following the vertical synchronization pulse associated with the second frame.

14. (Previously Presented) The system of claim 13, wherein the controller overwrites the information regarding the first frame with the information regarding the second frame and wherein the rasterizing circuit rasterizes the second frame based on the information regarding the second frame.

15-20. (Cancelled)

21. (Currently Amended) The system of claim 13, wherein the rasterizing circuit rasterizes the second frame, if the controller ~~does~~ provides the information regarding the second frame to the rasterizing circuit after the vertical synchronization pulse associated with the second frame and before ~~a~~ the first horizontal synchronization pulse following ~~a~~ the vertical synchronization pulse associated with the second frame.